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PEARL COHEN ZEDEK, LLP 1500 BROADWAY 12TH FLOOR NEW YORK, NY 10036			BLEVINS, JERRY M	
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Please find below and/or attached an Office communication concerning this application or proceeding.

DETAILED ACTION

Response to Arguments

Applicant's arguments filed April 20, 2006 have been fully considered but they are not persuasive.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Specifically, although neither applied prior art references, those of DiJaili et al., US 6,765,715 and Patel et al., US 2001/0015842, individually teach the combination of an optical chopping device including an optical splitter and an all-optical AND logic gate, the combination of these references, as applied in the below 103 obvious-type rejection does teach this combination.

Furthermore, applicants assert that the splitter of Patel is associated with only one input of the AND gate of Patel. Examiner respectfully disagrees with this assertion. Patel, in paragraphs 55-57, page 3, teaches that input ports 86 and 98 (Figure 3) are each associated with splitter 88.

In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon

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hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

In the present case, examiner did not solely glean knowledge from applicant's disclosure. Justification for examiner's motivation to combine can be found on page 1, paragraph 9 of Patel, where Patel teaches that the structure of a splitter with that of an AND gate increases reliability and accuracy of the AND gate.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-3, 10-12, and 16-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over DiJaili in view of Patel.

Regarding claim 1, DiJaili teaches an all optical chopping device for shaping and reshaping (Figure 1) comprising an all optical AND logic gate (108, 116 and shown in Figure 10) having a first and second inputs (A, B) and at least one output (X), wherein one of said first and second inputs includes an optical delay line (column 15, line 5 – column 16, line 6), wherein said AND gate is arranged to produce at said output an

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optical output signal corresponding to a portion of the AND product of said first optical signal component and said second optical signal component (column 12, line 26 – column 14, line 4), said optical output signal being narrower than said optical input signal (Figures 2-4). DiJaili does not teach an optical splitter having an input terminal and first and second output terminals, wherein the input terminals of the AND gate are associated with the output terminals of the splitter, wherein the splitter is arranged to receive an optical input signal from the input terminal and to split the optical input signal into first and second optical signal components to exit at the first and second output terminals, wherein the AND gate is arranged to receive the first and second optical signal components via the first and second inputs. Patel teaches an optical AND gate (Figure 3, 80) comprising a splitter (88) having an input terminal (86) and first and second output terminals (86,96, page 5, paragraphs 55-57), wherein the input terminals of the AND gate (86, 98) associated with the output terminals of the splitter (paragraphs 55-57) wherein the splitter is arranged to receive an optical input signal (82) from the input terminal and to split the optical input signal into first and second optical signal components (90, 92) to exit at the first and second output terminals wherein the AND gate is arranged to receive the first and second optical signal components via the first and second inputs (Figure 3, paragraphs 55-57). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify DiJaili with the splitter of Patel. The motivation would have been to improve the reliability and accuracy of the AND gate (Patel, page 1, paragraph 9).

Regarding claim 2, DiJaili teaches that said first optical signal component and said second optical signal component are delayed relative to each other (Figures 2-4).

Regarding claim 3, DiJaili teaches that said delay is shorter than one of said first optical signal component and said second optical signal component (Figures 2-4).

Regarding claim 10, DiJaili in view of Patel teaches the limitations of the base claim 1. DiJaili does not teach that one of said first second inputs of the optical AND gate includes an optical amplifier. Patel teaches an optical AND gate wherein one of a first input and a second input includes an optical amplifier (Figure 4, element 132). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify DiJaili with the amplifier of Patel. The motivation would have been to increase the amount of signals which could utilize the AND gate.

Regarding claim 11, DiJaili in view of Patel teaches the limitations of the base claim 1. DiJaili does not teach a closed loop phase control. Patel teaches an optical AND gate comprising a closed loop phase control (Figure 3 and page 5, paragraph 56). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify DiJaili with the closed loop phase control of Patel. The motivation would have been to improve the reliability and accuracy of the AND gate.

Regarding claim 12, DiJaili in view of Patel teaches the limitations of the base claim 1. DiJaili does not teach a closed loop synchronization control. Patel teaches an optical AND gate comprising a closed loop synchronization control (Figure 3 and page 5, paragraph 56). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify DiJaili with the closed loop synchronization control of

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Patel. The motivation would have been to improve the reliability and accuracy of the AND gate.

Regarding claim 16, DiJaili teaches that said first optical signal component and said second optical signal component are coherent (column 12, line 26 – column 14, line 4, which teach that the sources are lasers, which produce coherent light).

Regarding claim 17, DiJaili in view of Patel teaches the limitations of the base claim 1. DiJaili does not teach that said AND logic gate includes a summing gate selected from the group of summing gates containing beam splitters, dielectric beam splitters, metallic beam splitters, dual gratings, interleaved arrayed of waveguides, and dense dual gratings. Patel teaches an AND logic gate including a summing gate containing beam splitters (page 5, paragraph 55). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify DiJaili with the beam splitter of Patel. The motivation would have been to improve the reliability and accuracy of the AND gate.

Regarding claim 18, DiJaili teaches that said AND logic gate includes a threshold device (Figure 1, flop-flop 104).

Regarding claim 19, DiJaili in view of Patel teaches the limitations of the base claim 1. DiJaili does not teach that said AND logic gate includes an optical loop. Patel teaches an AND logic gate including an optical loop (page 5, paragraph 55). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify DiJaili with the optical loop of Patel. The motivation would have been to improve the reliability and accuracy of the AND gate.

Regarding claim 20, DiJaili in view of Patel teaches the limitations of the base claim 1. DiJaili does not teach that said AND logic gate includes a non-linear optical loop. Patel teaches an AND logic gate including a non-linear optical loop (page 5, paragraph 55). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify DiJaili with the non-linear optical loop of Patel. The motivation would have been to improve the reliability and accuracy of the AND gate.

Claims 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over DiJaili in view of Patel as applied to claim 1 above, and further in view of US Patent to Jensen, number 4,632,518.

Regarding claims 13 and 14, DiJaili in view of Patel teaches the limitations of the base claim 1. DiJaili does not teach that said optical output signal is produced by head or tail chopping of said optical input signal. Jensen teaches an optical AND gate wherein an optical output is produced by chopping an optical input signal at an appropriate location, which would include head and tail chopping (column 8, lines 40-56). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify DiJaili with the appropriately located chopping of Jensen. The motivation would have been to improve reliability and accuracy of the phase shifting of the signals (column 8, lines 40-56).

Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over DiJaili in view of Patel as applied to claim 1 above, and further in view of US Patent to Byun et al., number 6,804,047.

Regarding claim 21, DiJaili in view of Patel teaches the limitations of the base claim 1. DiJaili does not teach that the optical delay line is a variable optical delay line. Byun teaches an all-optical gate employing a variable optical delay line (Figure 1, column 2, line 47 – column 3, line 13, and column 3, line 58 – column 4, line 27). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify DiJaili with the variable optical delay line of Byun. The motivation would have been to allow for greater control over the delay.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

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the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jerry Martin Blevins whose telephone number is 571-272-8581. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Frank G. Font can be reached on 571-272-2415. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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